Patent claims

1. A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising the following method steps:

A) provision of a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on the semiconductor surface;

B) production of an insulator layer on the semiconductor surface;

C) formation of a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) formation of material plugs on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks;

E) anisotropic etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) production of a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching of sacrificial layer material from the vitreous layer for the purpose of removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removal of the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling of the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer.

2. The method as claimed in claim 1, method step F) comprising the following method steps:

F1) removal of the material plugs;

F2) removal of the uncovered insulator layer on the semiconductor surface between the mutually adjacent gate electrode tracks;

F3) production of dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for the purpose of forming the selection transistors;

F4) production of a liner layer, which preferably comprises silicon nitride;

F5) formation of the vitreous layer on the liner layer, the regions between the mutually adjacent gate electrode tracks essentially being filled; and

F6) planarization of the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the essentially planar surface being formed.

3. The method as claimed in claim 2, the liner layer being a nitrogen-containing layer, preferably silicon nitride layer or a silicon oxide-nitride layer.

4. The method as claimed in claim 2 or 3, the planarization in method step F6) being effected by chemical mechanical polishing and the end point of the polishing operation being defined at the establishment of a material removal of the liner layer.

5. The method as claimed in one of claims 1 to 4, the vitreous layer formed in method step F) being a BPSG layer.

6. The method as claimed in one of claims 1 to 5, method step C) comprising the following method steps:
C1) deposition of a first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;
C2) planarization of the first sacrificial layer with uncovering of the gate electrode tracks, an essentially planar surface being formed; and
C3) deposition of a second sacrificial layer.

7. The method as claimed in claim 6, the second sacrificial layer having a layer thickness of 200 nm to 1000 nm.

8. The method as claimed in one of claims 1 to 5, method step C) comprising the following method steps:
C1') deposition of the sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks being filled and the gate electrode tracks being covered; and
C2') planarization of the sacrificial layer, the gate electrode tracks remaining covered and an essentially planar surface being formed.

9. The method as claimed in claim 8, the sacrificial layer having a layer thickness of 200 nm to 1000 nm above the gate electrode tracks.

10. The method as claimed in one of claims 1 to 9, the insulator layer being a silicon dioxide layer.

11. The method as claimed in one of claims 1 to 10, method step D) comprising the following method steps:

D1) deposition of a resist layer;

D2) exposure of the resist layer by means of a mask which defines the contact openings between the mutually adjacent gate electrode tracks; and

D3) development of the resist layer in order to remove the exposed regions of the resist layer and to form the material plugs made from resist material on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks.

12. The method as claimed in claim 11, an ARC layer being applied on the sacrificial layer before the resist layer.

13. The method as claimed in one of claims 1 to 10, method step D) comprising the following method steps:

D1') deposition of a hard mask layer on the sacrificial layer;

D2') deposition of a resist layer on the hard mask layer;

D3') exposure of the resist layer by means of a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D4') development of the resist layer in order to remove the exposed regions of the resist layer outside the contact openings between the mutually adjacent gate electrode tracks;

D5') anisotropic etching of the hard mask layer with the patterned resist layer as a mask; and

D8') removal of the residual resist layer.

14. The method as claimed in one of claims 1 to 10, method step D) comprising the following method steps:

D1'') formation of a hard mask layer on the sacrificial layer;

D2'') planarization of the hard mask layer;

D3'') deposition of a resist layer on the hard mask layer;

D4'') exposure of the resist layer by means of a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D5'') development of the resist layer in order to remove the exposed regions of the resist layer and to uncover the hard mask layer;

D6'') anisotropic etching of the hard mask layer with the patterned resist layer as a mask;

D7'') removal of the patterned resist layer;

D8'') introduction of a filling material into the etching openings in the hard mask layer; and

D9'') removal of the hard mask layer in order to form the material plugs made from the filling material on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks.

15. The method as claimed in claim 14, the hard mask layer being a vitreous layer, preferably a BPSG layer, and the filling material being an organic ARC material.

16. The method as claimed in one of claims 1 to 15, the sacrificial layer being a polysilicon layer.

17. The method as claimed in one of claims 1 to 16, the sacrificial layer being a carbon layer.

18. The method as claimed in claim 17, a dielectric hard mask layer additionally being provided on the carbon layer.

19. A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising the following method steps:

A) provision of a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on the semiconductor surface;

B) production of an insulator layer on the semiconductor surface;

C) formation of a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) formation of material plugs on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks;

E) anisotropic etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) production of a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching of sacrificial layer material from the vitreous layer for the purpose of removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removal of the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling of the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

method step C) comprises the following method steps:

C1') deposition of a first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

C2') planarization of the first sacrificial layer with uncovering of the gate electrode tracks, an essentially planar surface being formed; and

C3') deposition of a second sacrificial layer.

20. The method as claimed in claim 19, wherein the second sacrificial layer has a layer thickness of 200 nm to 1000 nm.

21. A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising the following method steps:

A) provision of a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on the semiconductor surface;

B) production of an insulator layer on the semiconductor surface;

C) formation of a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) formation of material plugs on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks;

E) anisotropic etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) production of a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching of sacrificial layer material from the vitreous layer for the purpose of removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removal of the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling of the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

method step C) comprises the following method steps:

C1'') formation of a plane first sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered; and

C3'') deposition of a hard mask layer formed as a second sacrificial layer.

22. The method as claimed in one of claims 19 to 21, wherein method step D) comprises the following method steps:

D1') deposition of a resist layer;

D2') exposure of the resist layer by means of a mask which defines the contact openings between the mutually adjacent gate electrode tracks; and

D3) development of the resist layer in order to remove the exposed regions of the resist layer and to form the material plugs made from resist material on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks.

23. The method as claimed in claim 22, wherein an ARC layer is applied on the sacrificial layer before the resist layer.

24. A method for fabricating a first contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, comprising the following method steps:

A) provision of a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on the semiconductor surface;

B) production of an insulator layer on the semiconductor surface;

C) formation of a sacrificial layer on the insulator layer, the regions between the mutually adjacent gate electrode tracks essentially being filled and the gate electrode tracks being covered;

D) formation of material plugs on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks;

E) anisotropic etching of the sacrificial layer, the material plugs with the underlying sacrificial layer blocks remaining;

F) production of a vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the regions between the mutually adjacent gate electrode tracks essentially being filled and an essentially planar surface being formed;

G) etching of sacrificial layer material from the vitreous layer for the purpose of removing the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks;

H) removal of the uncovered insulator layer above the contact openings on the semiconductor surface between the mutually adjacent gate electrode tracks; and

I) filling of the contact opening regions with a conductive material, in the process forming an essentially planar surface with the surrounding vitreous layer,

wherein

method step D) comprises the following method steps:

D1') formation of a hard mask layer on the sacrificial layer;

D2'') planarization of the hard mask layer;

D3'') deposition of a resist layer on the hard mask layer;

D4'') exposure of the resist layer by means of a mask which defines the contact openings between the mutually adjacent gate electrode tracks;

D5'') development of the resist layer in order to remove the exposed regions of the resist layer and to uncover the hard mask layer;

D6'') anisotropic etching of the hard mask layer with the patterned resist layer as a mask;

D7'') removal of the patterned resist layer;

D8'') introduction of a filling material into the etching openings in the hard mask layer; and

D9'') removal of the hard mask layer in order to form the material plugs made from the filling material on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks.

25. The method as claimed in claim 24, wherein the hard mask layer is a vitreous layer, preferably a BPSG layer, and the filling material is an organic ARC material.

26. The method as claimed in one of claims 19 to 25, wherein the insulator layer is a silicon dioxide layer.

27. The method as claimed in one of claims 19 to 26, wherein method step F) comprises the following steps:

F1) removal of the material plugs;

F2) removal of the uncovered insulator layer on the semiconductor surface between the mutually adjacent gate electrode tracks;

F3) production of dopings in predetermined regions of the uncovered semiconductor surface between the mutually adjacent gate electrode tracks for the purpose of forming the selection transistors;

F4) production of a liner layer;

F5) formation of the vitreous layer on the liner layer, the regions between the mutually adjacent gate electrode tracks essentially being filled; and

F6) planarization of the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, the essentially planar surface being formed.

28. The method as claimed in claim 27, wherein the liner layer is a nitrogen-containing layer, preferably silicon nitride layer or a silicon oxide-nitride layer.

29. The method as claimed in claim 27 or 28, wherein the planarization in method step F6) is effected by chemical mechanical polishing and the end point of the polishing operation is defined at the establishment of a material removal of the liner layer.

30. The method as claimed in one of claims 19 to 29, the vitreous layer formed in method step F) being a BPSG layer.